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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/818,788	03/28/2001	Ayman G. Abdo	2207/10611	1020

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EXAMINER	
MANOSKEY, JOSEPH D	
ART UNIT	**PAPER NUMBER**
2113	

DATE MAILED: 04/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/818,788	ABDO ET AL.	
	Examiner	Art Unit	
	Joseph Manoskey	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5-10 and 18-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5,7,18,20-29,33,36 and 37* is/are rejected.

7)☒ Claim(s) *6,8-10,19,30-32,34 and 35* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see page 9, second paragraph, filed in Amendment B on February 10, 2004, with respect to the specification have been fully considered and are persuasive. The objection of the specification has been withdrawn.

2. Applicant's arguments, see page 8, third paragraph, filed in Amendment B on February 10, 2004, with respect to claim 9 have been fully considered and are persuasive. The rejection under 35 U.S.C. 112 of claim 9 has been withdrawn.

3. Applicant's arguments, see page 10, section A, filed in Amendment B on February 10, 2004, with respect to the rejection(s)of claim(s) 5-10 under 35 U.S.C. 102(e) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of new prior art (See below for rejection).

4. Applicant's arguments, see page 10 and 11 section B, filed in Amendment B on February 10, 2004, with respect to the rejection(s)of claim(s) 18 and 19 under 35 U.S.C. 102(e) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of new prior art (See below for rejection).

Claim Objections

5. Claim 33 is objected to because of the following informalities: on the last line the claim recites "harassing instruction", it is believed that the claim should recite "harassing transaction" and will be interpreted as such for the purposes of further examination. Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claim 18 is rejected under 35 U.S.C. 102(b) as being anticipated by Gates, U.S. Patent 5,701,409.

8. Referring to claim 18, Gates teaches generating errors, or injecting faults, on a bus for testing purposes, this is interpreted as stress testing for a computer system (See Col. 2, lines 35-46). Gates also discloses waiting until enough time has past to assert

an error signal on the bus (See Col. 7, lines 17-24). In order to wait an elapsed amount of time on a digital computer a counting of cycles is used and it is interpreted that the error signal is not asserted high until after a number of cycles from the bus have been counted. Gates finally teaches, after the time has elapsed, generating an error signal, that injects a fault onto the bus, this is interpreted as generating a harassing transaction on the bus (See Col. 7, lines 17-24 and 59-65).

9. Claims 20-23, 29, and 33 are rejected under 35 U.S.C. 102(e) as being anticipated by Coyle et al., U.S. Patent 6,609,221, hereinafter referred to as "Coyle".

10. Referring to claim 20, Coyle teaches an integrated circuit that includes core logic, and bus testing logic coupled to external bus interface, which are interpreted as a processor core and a validation FUB (See Fig. 1). Although Coyle does not express the core logic having a clock, it is inherent that the core logic operates in the domain of a clock and Coyle shows the bus testing logic connected with core logic, this is interpreted as the validation FUB operating in the domain of the clock from the core logic (See Fig. 1 and 4A). Coyle discloses the testing logic of including the additional function to arbitrate for control of the bus, this is interpreted as a data request pipeline, and Coyle shows the device including a bus interface (See Col. 4, lines 6-8 and Fig. 8). Finally Coyle teaches the bus having its own clock (See Fig. 3).

11. Referring to claim 21, Coyle testing the bus by deterministic saturations of the bus which induce errors, such as system-level bottlenecks, it is interpreted that bottleneck is caused by the nature of the bus clock being slower than the core logic clock (See Col 4, lines 31-35).

12. Referring to claim 22, Coyle teaches the validation FUB comprising a pattern storage, which is interpreted as a transaction latch, coupled to the bus interface (See Fig. 4A and Col. 7, line 34-35). Coyle also teaches a pattern source, interpreted as a request library, in communication with the transaction latch and coupled to the bus interface (See Fig. 4A and Col. 7, line 32-34).

13. Referring to claim 23, Coyle teaches the pattern source can also include a pattern generator, this is interpreted as an address manipulator, which is attached to the request library and the bus interface (See Col. 9, lines 35-37).

14. Referring to claim 29, Coyle teaches a testing method of a receiver end storing a received pattern, this is interpreted as detecting an onset of a first transaction (See Col. 6, lines 9-14). Coyle also teaches generating a replica version and sending it over the bus, which is interpreted as reading the address and sending a transaction on the bus directed to the same address as the first transaction (See Col. 6, lines 21-26).

15. Referring to claim 33, Coyle teaches a testing method of a receiver end storing a received pattern, this is interpreted as detecting an onset of a first transaction (See Col. 6, lines 9-14). Coyle also teaches generating a replica version and sending it over the bus, which is interpreted as reading the address and sending a transaction on the bus directed to the same address as the first transaction (See Col. 6, lines 21-26). The replica version of the transaction is interpreted as a harassing transaction.

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 5, 7, 24-26, 36, and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coyle in view of De Angelis et al., U.S. Patent 5,142,673, hereinafter referred to as "De Angelis".

18. Referring to claim 5, Coyle teaches stress testing (See Col. 4, lines 26-38). Coyle discloses capturing a bus transaction, and upon meeting a loop-back condition generating an echo cycle (See Fig. 2B), the echo cycle is interpreted as a harassing bus transaction. Coyle does not teach generating a data request if the transaction meets a trigger condition, however Coyle does disclose a loop-back mode to determine if the

echo should be transmitted (See Fig. 5). De Angelis teaches a bus including trigger generating means for storing patterns when a trigger condition is meet (See Col. 2, lines 13-16). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the echoing of transactions of Coyle with the trigger generating means of De Angelis. This would have been obvious to one of ordinary skill in the art at the time of the invention to do because it allows the user to select specific conditions to be detected (See De Angelis, Col. 1, lines 48-51 and Col. 2, lines 28-33).

19. Referring to claim 7, Coyle and De Angelis teach all the limitations (See rejection of claim 5) including the echo cycle or harassing bus transaction being a replica version of the captured bus transaction (See Coyle, Col. 6, lines 21-25), this is interpreted as the echo cycle bus transaction containing the same address as the first bus transaction.

20. Referring to claim 24, Coyle teaches an integrated circuit that includes core logic, and bus testing logic coupled to external bus interface, which are interpreted as a processor core and a validation FUB (See Fig. 1). Coyle discloses the testing logic of including the additional function to arbitrate for control of the bus, this is interpreted as a bus sequencing unit with an arbiter, and Coyle shows the device including a bus interface (See Col. 4, lines 6-8 and Fig. 8). Coyle also discloses the device having pattern storage, this is interpreted as cache to store data (See Fig. 4A). Coyle teaches the device having queues in the bus interface with is in communication with device, this is interpreted as transactions queues (See Fig. 4A). Coyle does not teach generating a

data request if the transaction meets a trigger condition, however Coyle does disclose a loop-back mode to determine if the echo should be transmitted (See Fig. 5). De Angelis teaches a bus including trigger generating means for storing patterns when a trigger condition is meet (See Col. 2, lines 13-16). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the echoing of transactions of Coyle with the trigger generating means of De Angelis. This would have been obvious to one of ordinary skill in the art at the time of the invention to do because it allows the user to select specific conditions to be detected (See De Angelis, Col. 1, lines 48-51 and Col. 2, lines 28-33).

21. Referring to claim 25, Coyle and De Angelis teach all the limitations (See rejection of claim 24) including the validation FUB being coupled to the arbiter (See Coyle, Fig. 4A).

22. Referring to claim 26, Coyle and De Angelis teach all the limitations (See rejection of claim 25) including the data request and second data request being processed as independent transactions. Coyle teaches the echo cycle being generated after gaining control of the driver (See Col. 6, lines 21-26). This means that echo cycle or second data request is processed independent of the first one.

23. Referring to claim 36, Coyle teaches a testing method of a receiver end storing a received pattern, this is interpreted as observing a transaction on an external bus (See

Col. 6, lines 9-14). Coyle also teaches generating a replica version and send it over the bus, which is interpreted as generating a transaction in response to first transaction (See Col. 6, lines 21-26). Coyle does not teach storing a type in a register and generating the transaction in response to the type of observing the first transaction, however Coyle does disclose a loop-back mode to determine if the echo should be transmitted (See Fig. 5). De Angelis teaches a bus including trigger generating means for storing patterns when a trigger condition is meet, the trigger is interpreted as a match of the type of the transaction (See Col. 2, lines 13-16). De Angelis also teaches the use of a trigger register (See Fig. 2). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the echoing of transactions of Coyle with the trigger generating means of De Angelis. This would have been obvious to one of ordinary skill in the art at the time of the invention to do because it allows the user to select specific conditions to be detected (See De Angelis, Col. 1, lines 48-51 and Col. 2, lines 28-33).

24. Referring to claim 37, Coyle and De Angelis teach all the limitations (See rejection of claim 37) including generating a harassing bus transaction based on the data request. Coyle discloses generating a replica version and sending it over the bus, which is interpreted as generating a harassing transaction in response to the data request (See Col. 6, lines 21-26).

25. Claims 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coyle, in view of De Angelis and Westcott et al., U.S. Patent 5,151,981, hereinafter referred to as "Westcott".

26. Referring to claim 27, Coyle teaches an integrated circuit that includes core logic, and bus testing logic coupled to external bus interface, which are interpreted as a processor core and a validation FUB (See Fig. 1). Coyle discloses the testing logic of including the additional function to arbitrate for control of the bus, this is interpreted as a bus sequencing unit with arbiter, and Coyle shows the device including a bus interface (See Col. 4, lines 6-8 and Fig. 8). Coyle also discloses the device having pattern storage, this is interpreted as cache to store data (See Fig. 4A). Coyle teaches the device having queues in the bus interface with is in communication with device, this is interpreted as transactions queues (See Fig. 4A). Coyle does not teach generating a data request if the transaction meets a trigger condition from a hit/miss signal from the cache, however Coyle does disclose a loop-back mode to determine if the echo should be transmitted and the desire for inducing system-level bottlenecks for testing purposes (See Fig. 5 and Col. 4, lines 31-35). De Angelis teaches a bus including trigger generating means for storing patterns when a trigger condition is meet (See Col. 2, lines 13-16). Westcott discloses using cache hit/miss data for meeting trigger conditions (See Col. 5, lines 13-27). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the echoing of transactions of Coyle with the trigger generating means of De Angelis and the cache hit/miss for triggering of

Westcott. This would have been obvious to one of ordinary skill in the art at the time of the invention to do because it allows the user to select specific conditions to be detected (See De Angelis, Col. 1, lines 48-51 and Col. 2, lines 28-33) and because the cache hit/miss signal allows for system bottlenecks to be identified (See Westcott, Col. 1, lines 14-20).

27. Referring to claim 28, Coyle, De Angelis, and Westcott teach all the limitations (See rejection of claim 27) including the trigger condition being whether the requested data is present in cache memory. Westcott discloses using cache hit/miss data for meeting trigger conditions; this is interpreted as the data concerning the trigger condition being located in the cache (See Col. 5, lines 13-27).

Allowable Subject Matter

28. Claims 6, 8-10, 19, 30-32, 34, and 35 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Manoskey whose telephone number is (703) 308-5466. The examiner can normally be reached on Mon.-Fri. (8am to 4:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JDM
March 30, 2004

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